An Area Efficient and Reusable HEVC 1D-DCT Hardware Accelerator

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In this paper is presented an area efficient reusable architecture for integer one dimensional Discrete Cosine Transform (1D DCT)with adjustable transform sizes in High Efficiency Video Coding (HEVC). Optimization is based on exploiting of symmetry and subset properties of the transform matrix. The proposed multiply-add architecture is fully pipelined and applicable for all transform sizes. It provides the interface over which the processing system can control the datapath of the transform process and the synchronization channel that enables the system to receive the feedback information about utilization from the device. An intuitive line approach for calculating transform coefficients for all transform sizes was used instead of the commonly applied recursive decomposition approach. This approach simplifies disabling of lines that are not employed for a particular transform size. The proposed architecture is implemented on the FPGA platform, can operate at 406,3 MHz,achieves throughput of 812,7 Msps and can support encoding of a 4K UHD@30fps video sequence in real time.

Keywords: Integer discrete cosine transform (DCT), High Efficiency Video Coding (HEVC), Field-programmable gate array (FPGA), Pipelined architecture.