A new hardware counters based thread migration strategy for NUMA systems

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Multicore systems present on-board memory hierarchies and communication networks that influence performance when executing shared memory parallel codes. Characterising this influence is complex, and understanding the effect of particular hardware configurations on different codes is of paramount importance. In this paper, monitoring information extracted from hardware counters at runtime is used to characterise the behaviour of each thread in the processes running in the system. This characterisation is given in terms of number of floating point operations per second, operational intensity, and latency of memory access. We propose to use this information to guide a thread migration strategy that improves execution efficiency by increasing locality and affinity. Different configurations of NAS Parallel OpenMP benchmarks on multicores were used to validate the benefits of the proposed thread migration strategy. Our strategy produces up to 70% improvement in scenarios where locality and affinity are low, being the degradation in performance low for codes with high locality and affinity.

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