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2013

SPECIAL SESSION ON MULTICORE SYSTEMS

th International Conference on

Parallel Processing and Applied Mathematics

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Warsaw, Poland September 8-11, 2013

Warsaw, POLAND 52.259 °N 21.020 °E

Since future technologies offer the promise of being able to integrate billions of transistors on a chip, the prospects of having hundreds of processors on a single chip along with an underlying memory hierarchy and an interconnection system is entirely feasible. Multicore architectures have already made their way in the industry, with more aggressive configurations, called manycore architectures, being prototyped.

While these systems have a potential of providing significant performance benefits, it is a major challenge to exploit the available resources in multicore/manycore architectures. Starting from gate-level implementations all the way to application implementation, there are multiple dimensions that need to be considered for effective implementation and usage of such architectures.

SPECIAL SESSION SCOPE

This special session aims to provide a forum for researchers and engineers to present new ideas in the multicore/manycore field and discuss challenges and opportunities to improve multicore/manycore system effectiveness. Authors are invited to submit high quality papers representing original work in (but not limited to) the following topics:

- Multicore/manycore architectures: design, implementation, case studies
- Programming paradigms
- Parallel programming for multicore/manycore
- Compiler optimizations targeting multicore/manycore
- Memory hierarchy, last level cache management
- Thermal and temperature aware architectures
- Embedded multicore architectures
- Reliability-aware multicore design
- System-on-chip
- Network-on-Chip

SESSION CHAIRS

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SPECIAL SESSION COMMITTEE

TBD

IMPORTANT DATES

Submission of Papers May 15, 2013 Notification of Acceptance June 15, 2013 Camera-Ready Papers Nov. 15, 2013

CONTACT INFORMATION

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